WHAT IS CLAIMED IS:

1. A semiconductor memory device comprising:

a memory array including a plurality of memory cells arranged in rows and columns;

main control circuitry for producing a plurality of main control signals having different phases in response to a row-related instructing signal instructing an operation related to row selection in said memory array; and

sub-control circuitry receiving said plurality of main control signals, for producing sub-control signals greater in number than said plurality of main control signals, said sub-control signals being signals for controlling the operation instructed by said row-related instructing signal.

2. The semiconductor memory device according to claim 1, further comprising a plurality of banks activated independently of each other, wherein

said plurality of main control signals are independent of a signal specifying a bank among said plurality of banks.

3. The semiconductor memory device according to claim 1, wherein

said main control circuitry includes a plurality of control signal generating circuits activated sequentially to produce said plurality of main control signals in response to said row-related instructing signal.

4. The semiconductor memory device according to claim 1, wherein

said memory array is divided into a plurality of memory blocks each having a plurality of memory cells,

said sub-control circuitry includes a plurality of sub-control circuits provided corresponding to said plurality of memory blocks, and

said plurality of main control signals are transferred to said plurality of sub-control circuits with a same line load, respectively.

5. The semiconductor memory device according to claim 1, wherein said main control circuitry includes:

a first control circuit for activating a first main control signal in response to a row selection instruction by said row-related instructing signal,

a second control circuit for activating a second main control signal in response to activation of said first main control signal, and deactivating said second main control signal in response to deactivation of said first main control signal, and

a third control circuit for activating a third main control signal in response to activation of said second main control signal, and deactivating said third main control signal in response to deactivation of said second main control signal; and

said first control circuit deactivates said first main control signal in response to activation of said third main control signal.

6. The semiconductor memory device according to claim 5, further comprising:

a first delay circuit arranged between the first and second control circuits, for delaying said first main control signal for application to said second control circuit;

a second delay circuit arranged between the second and third control circuits for delaying said second main control signal for application to said third control circuit; and

a third delay circuit arranged between the third and first control circuits for delaying activation of said third main control signal for application to said first control circuit.

7. The semiconductor memory device according to claim 6, wherein the first, second and third delay circuits have delay times set individually and independently.

8. The semiconductor memory device according to claim 1, further

comprising:

an address input circuit for taking in and buffering an externally applied address signal to produce an internal address for application to said sub-control circuitry.

9. The semiconductor memory device according to claim 8, wherein

said memory array is divided into a plurality of memory blocks each having a plurality of memory cells,

said sub-control circuitry includes a plurality of sub-control circuits provided corresponding to said plurality of memory blocks, respectively,

each of said plurality of sub-control circuits includes a block decode circuit for receiving and decoding a plurality of block address bits included in said internal address, and

said block decode circuit includes;

an input circuit for producing complementary address bits from each of said block address bits,

a switch circuit for selecting one of said complementary address bits for each block address bit, and

a decode circuit for decoding address bits received from the switch circuit to produce a block select signal for selecting a corresponding memory block.

10. The semiconductor memory device according to claim 1, wherein

said memory array is divided into a plurality of memory blocks each having a plurality of memory cells,

said sub-control circuitry includes a plurality of sub-circuits provided corresponding to said plurality of memory blocks, respectively, and

each of said plurality of sub-control circuits includes;

a block decode circuit for decoding a block address included in said internal address to produce a block select signal specifying a corresponding memory block, and

a local control signal generating circuit for taking in the plurality of main control signals sent from said main control circuitry, and producing said plurality of sub-control signals when the block select signal generated from said block decode circuit is active.

11. The semiconductor memory device according to claim 10, wherein

each said sub-control circuit includes;

a first buffer circuit for taking in a first main control signal among said plurality of main control signals and producing a first internal main control signal in response to activation of said block select signal,

a second buffer circuit for taking in a second main control signal among said plurality of main control signals and producing a second internal main control signal in response to activation of said first internal main control signal received from said first buffer circuit, and

at least one buffer circuit provided corresponding to a remaining main control signal(s) among said plurality of main control signals for taking in a corresponding main control signal(s), and producing an internal main control signal(s) in response to activation of an internal main control signal on a preceding stage.

12. The semiconductor memory device according to claim 1, wherein

said main control circuitry includes a delay adjustment circuit for adjusting a delay between said plurality of main control signals, and

said sub-control circuitry produces said plurality of sub-control signals in accordance with the main control signals sent from said main control circuit and subjected to delay adjustment through the delay adjustment circuit.

13. The semiconductor memory device according to claim 1, wherein

said sub-control circuitry includes a switch circuit for changing a

relationship between said plurality of main control signals and said plurality of sub-control signals.

14. The semiconductor memory device according to claim 1, wherein

said main control circuitry includes a circuit for adjusting an active period of at least one of said plurality of main control signals in accordance with a test control signal activated in a test mode.

15. A semiconductor memory device comprising:

a plurality of memory blocks each having a plurality of memory cells, each of the memory cells requiring periodical refreshing of storage data;

refresh address generating circuitry for generating a refresh address signal designating a memory cell to be refreshed in accordance with a refresh instruction instructing refreshing of data of the memory cell in the memory blocks, said refresh address signal including a refresh block address signal designating a memory block to be refreshed among said plurality of memory blocks; and

block select circuits arranged corresponding to said plurality of memory blocks, each for producing a refresh block select signal indicating whether a corresponding memory block is selected, in accordance with said refresh block address signal, and

said refresh address generating circuitry including a reset signal producing circuit for producing a reset signal for resetting said refresh block address signal to an initial value in accordance with at least said refresh block select signal.

16. The semiconductor memory device according to claim 15, wherein

said refresh address generating circuitry includes:

a refresh block address producing circuit for producing said refresh block address signal such that said plurality of memory blocks are

refreshed in a predetermined sequence; and

a refresh word line address generating circuit for producing a word line address signal successively designating rows of memory cells in each of the memory blocks, the memory cells being arranged in rows and columns in each of said memory blocks, and word lines being arranged corresponding to the rows of memory cells, and

said reset signal producing circuit produces said reset signal in response to the refresh block select signal applied from a final memory block in said predetermined sequence of said plurality of memory blocks, and a final word line address signal, designating a final word line in a word line selection sequence, applied from said word line address generating circuit and said refresh instruction.

17. The semiconductor memory device according to claim 15, wherein

said plurality of memory blocks are refreshed in a predetermined refresh sequence in accordance with the refresh address signal, and

said reset signal producing circuit detects completion of the refresh for a final memory block in the refresh sequence of said plurality of memory blocks, for producing said reset signal.

18. The semiconductor memory device according to claim 15, wherein

said block select circuits each include:

a refresh block decoder for producing the block select signal for a corresponding memory block in accordance with the refresh block address signal applied from said refresh address generating circuitry; and

said refresh block decoder includes:

a refresh complementary bit producing circuit for producing complementary address signal bits from a multi-bit internal address signal transmitted through an internal address signal bus, said refresh address signal generated from said refresh address generating circuitry being a multi-bit signal and being transmitted through said internal

signal bus;

an address select circuit for selecting the complementary address signal bits generated from said refresh complementary bit producing circuit in accordance with a select signal, and

a decode circuit for producing the block select signal for the corresponding memory block in accordance with selected address signal bits applied from said address select circuit.

19. The semiconductor memory device according to claim 15, wherein

the memory cells are arranged in rows and columns in each of the memory blocks, and word lines are arranged corresponding to said rows,

said refresh address signal further includes a refresh word line address signal designating a word line in each of the memory blocks, and

said semiconductor memory device further comprises:

a refresh final word line detecting circuit arranged corresponding to each of said memory blocks for detecting whether a final word line in a refresh sequence is selected in the corresponding memory block in a refresh mode of refreshing memory cell data, and

a refresh word line reset signal generating circuit for producing a refresh word line reset signal resetting said refresh word line address signal to an initial value in accordance with a detection signal applied from said refresh final word line detecting circuit.

20. The semiconductor memory device according to claim 15, further comprising:

an address select circuit for receiving an external address signal and a refresh address signal generated from said refresh address generating circuit, transmitting said external address signal to an internal address signal bus when a normal operation mode instructing signal instructing a normal operation mode is active, and transmitting the refresh address signal generated from said refresh address generating circuit to said internal address signal bus when said normal operation mode instructing signal is inactive.